// **Half Subtractor**

module half\_sub(input ha,hb, output hby,hd);

assign hd = ha ^ hb;

assign hby = ~(ha) & hb;

endmodule

// **Full Subtractor**

module full\_sub(input a,b,c, output by,d);

wire x,y,z;

half\_sub hs1(a,b,x,y);

half\_sub hs2(y,c,z,d);

or(by,z,x);

endmodule

//**Testbench**

**module sub\_tb();**

**reg a,b,c;**

**wire by,d;**

**integer i;**

**full\_sub DUT(a,b,c,by,d);**

**initial**

**begin**

**$monitor("@time: %3d : a is %b, b is %b, c is %b where difference is %b and borrow is %b", $time, a,b,c,d,by);**

**for (i = 0 ; i <8 ; i = i+1)**

**begin**

**{a,b,c} = i;**

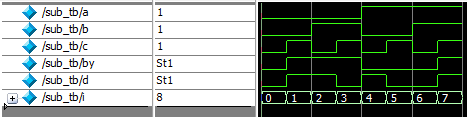
**#10;**

**end**

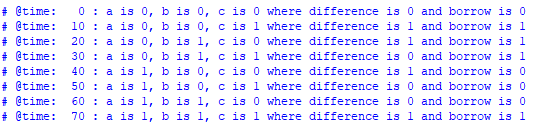
**end**

**endmodule**

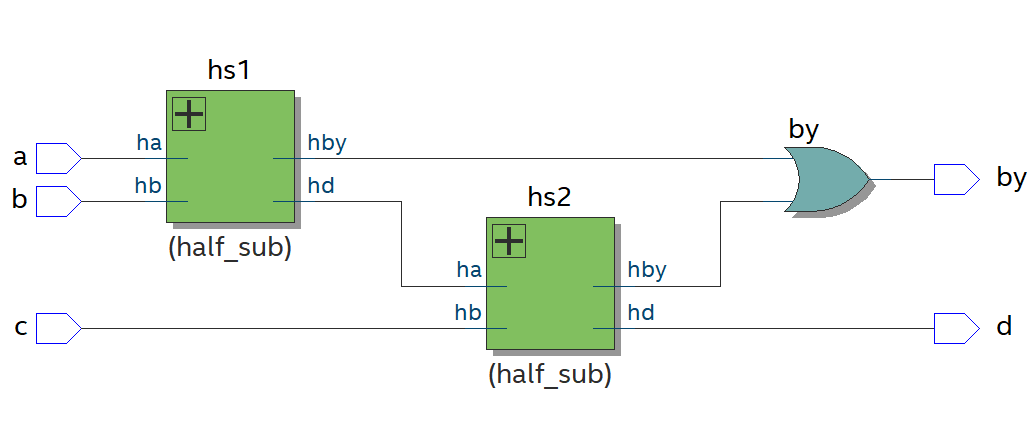
**Waveform:**

****

**Output:**

****

**RTL:**

****